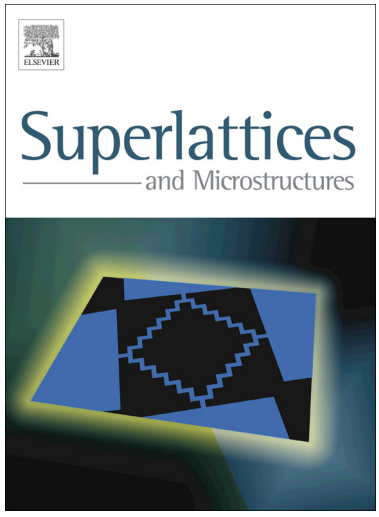

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Negative differential resistance in porous silicon devices at room temperature

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Abstract

We report a voltage controlled negative differential resistance (NDR) effect at room temperature in two types of devices based on porous silicon (PS): thermally oxidized porous silicon multilayer with Ag electrodes in a sandwich configuration (Ag/c-Si/PS/Ag) and porous silicon single layer with Al electrodes in a coplanar configuration (Al/PS/Al). The NDR effect was observed in current-voltage characteristics and showed telegraphic noise. The NDR effects showed a strong dependence with temperature and with the surrounding atmospheric air pressure. The NDR occurrence was attributed to the blocking of conduction channels due to carrier trapping phenomena. We also experimentally demonstrate porous silicon devices exploiting the NDR effect, with potential applications as volatile memory devices.

Keywords: Negative differential resistance; Porous silicon devices; Telegraphic noise; Coulomb repulsion.

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1. Introduction

Porous silicon (PS) has been one of the most studied materials in recent years [1, 2]; however, many of its properties do not have satisfactory explanation, remaining matter of debate. Among its interesting properties are quasibalistic electronic emission [3], electric-field induced switching of diode polarity[4], photoluminescence in the visible [5] and tunable optical properties [6]. In addition, due to its low cost of production and versatility, PS provides a wide range of technological applications.

The negative differential resistance (NDR) is a phenomenon of technological interest due to its multiple applications in electronics, such as in memory devices, oscillators and fast switching devices [7]. This effect was first observed in Esaki diodes [8] and in recent years it has been demonstrated in several semiconductor systems, including organic semiconductors [9], molecular nanowire junctions [10] and single electron devices [11]. Regarding silicon based devices, NDR has been observed also in amorphous silicon/silicon carbide devices [12], Si/SiO_2 nanowire, or quantum dot based devices [13] and also in porous silicon [14, 15].

The NDR effect is not associated with a single physical mechanism. A large variety of phenomena, such as tunneling [7], Coulomb blockade [13], charge storage [16], and other effects have been suggested as causes for the NDR. In this work, we discuss the NDR behavior observed in two different kinds of PS devices: 1) vertical, thermally-oxidized, PS multilayer structure, which has been reported as an efficient electron emitter [3], and 2) planar, single layer PS devices, which are being investigated as promising gas-sensors. Interestingly, both types of devices present very similar transport characteristics when

brought into the NDR state, which we attribute to a common dominant mechanism controlled by Coulomb repulsion effects.

We also propose a simple device that integrates PS structures to demonstrate the potential applications of their NDR phenomena in volatile memory devices.

2. Materials and Methods

All the PS-based devices studied in this paper (multilayer PS devices and single layer PS device) were prepared by electrochemical anodization of crystalline p-Si ($\rho = 2 - 4$ mΩ·cm) with <100> orientation.

In order to obtain PS multilayers with Ag electrodes in sandwich configuration, the crystalline silicon wafers were anodized in a 1:2 solution of HF (50%):Ethanol alternating high (60 mA/cm^2) and a low (20 mA/cm^2) current densities. This procedure resulted in alternate layers having two different porosities [6]. The etching process was designed to obtain structures with 8 layers of each porosity. As a result of the anodization process with high current densities layers with a porosity of 78% and a thickness of 86.1 nm were obtained, while for low current densities layers with a porosity of 60% and a thickness of 69.5 nm were obtained, so the total thickness of the multilayer samples was 1.25 µm. The top contact (Ag/SP) was deposited on the PS multilayer samples by electroless technique using a silver nitrate solution. The bottom contact (Ag/*c*-Si) was made with conductive silver paint. Finally, the devices were annealed at 300 °C for 5 minutes in air, a procedure that results in the formation of a 2 to 4 nm thick surface silicon oxide layer. [17]. We will name these structures in the text as Ag/c-Si/PS/Ag.

PS layers with Al electrodes in a co-planar configuration were also studied. These samples were fabricated by anodizing crystalline silicon wafers in a 1:2 solution of HF

(50%):Ethanol with a current density of 20 mA/cm^2. The resulting films are mesoporous (pore size of 5–10 nm) with porosity of 60% [4]. The anodization times were 200 s in order to obtain PS films with thicknesses of 2 µm. The PS films were separated from the silicon substrate by anodization in a 1:7 HF (50%):Ethanol solution using a short pulse of high current density (360 mA/cm^2). These PS layers were then transferred to glass slides previously coated with two aluminium contacts separated by a gap of 20µm. The transferred layers were dried under N_2 flow, forming mechanical Al/PS contacts. We will name these structures in the text as Al/PS/Al.

I-V experiments for Ag/c-Si/PS/Ag sandwich devices were made at atmospheric pressure and room temperature. Experiments with Al/PS/Al planar devices were made at 5x10^{-6} Torr, at different temperatures.

For detection of quasi-ballistic electrons, a metallic plate was placed at 10 mm from the sample surface. The device was placed into a vacuum chamber (1x10^{-5} Torr) and was biased between -20 V and 20 V, while the plate was maintained at a constant positive potential (100 V) during testing. The current in the plate had significant values (larger than the noise) only for positive biasing of the top contact with high enough voltages, as expected for electron emission.

3. Results and discussion

Figure 1(a) shows several I-V curves for the Ag/c-Si/PS/Ag multilayer obtained after several consecutive measurements. The first I-V curve shows no NDR region, but the successive curves change as indicated by the arrow, and start showing NDR for V > 3 V. For a sufficient large number of consecutive measurements, the I-V curves show a stationary behavior. Curves in Fig. 1(a) correspond to a sample having a contact area of 28

mm^2. Fig. 1(b) shows an I-V curve for a sample having much smaller contact area (0.2 mm^2) measured after several I-V cycles. As it can be observed in Fig. 1(b), this sample exhibits noisy behavior. However, somewhat stable states can be recognized, as indicated by the solid lines. The appearance of these states can be explained considering the existence of conduction channels with different resistance values extending through the PS device. This peculiar behavior may be associated with telegraph noise produced by the trapping and detrapping of carriers from traps located at the SiO_2/Si interface and the existence of silicon nanowires with different sizes due to an inhomogeneous oxidation process [18], which can lead to the blocking of conduction channels due to Coulomb repulsion [19]. The appearance of telegraph noise was confirmed by measuring the time-dependent current with a constant applied voltage (10 V), as shown in Fig. 1(c). As observed, the electric current showed a random behavior, with commutations between states having different resistance values, a characteristic behavior of telegraph noise.

Taking into account that the contact area of sample in Fig. 1(a) is about 140 times larger than the one in Fig. 1(b), the curves in Fig. 1(a) can be considered a resulting from 140 samples like that of Fig. 1(b) connected in a parallel configuration, so that the noisy behavior is averaged.

Quasi-ballistic transport has been reported in mesoporous silicon with mean free paths as long as 1.6 μm [3]. In our oxidized devices, we have also experimentally observed the existence of quasi-ballistic electrons as shown in Fig. 2. We assume that the quasi-ballistic electrons have enough energy to be trapped and localized into deep traps states near the Si/SiO_2 interface of the oxidized nanostructures. This leads to the electrostatic blocking of narrow conductive channels in the nanostructured silicon skeleton and consequently the appearance of NDR.

The freshly made Al/PS/Al devices did not evidence any NDR behavior, instead, the I-V curve exhibited a monotonically increasing electric current with increasing applied voltage and a hysteresis after cyclic voltage sweeps, as shown in Fig. 3(a). This hysteretic behavior was observed even after performing 15 consecutive I-V sweeps. In addition, the electric current showed a continued increase with time after applying a constant voltage without reaching a steady state even after almost two hours, as shown in Fig. 3(b). When the Al/PS/Al devices underwent several consecutive I-V cycles reaching high voltages (> 40 V), they switched into a highly conductive state (Inset of Fig. 3(a)). Note that the current was limited at 2.4 mA in order to preserve the integrity of the samples. After further successive I-V cycles (not shown), the sample remained in the same high conductivity state. After leaving the sample at zero bias during 3 hours, a new I-V experiment evidenced the existence of a NDR effect, as shown in Fig. 3(c). This new state, characterized by NDR, showed stability and irreversibility (i.e., it was not possible to recover the initial state of the sample, see Fig 3(a)). No NDR effect was observed for the case of samples that were not subjected to the high voltages. In that case, samples remained in the state shown in Fig. 3 (a).

Since a large voltage was applied before forming the NDR effect, it is conceivable that the temperature of the device was greatly increased due to the Joule effect, controlling the higher conductivity state shown in the inset of Fig. 3(a). Taking into account the highly probable existence of residual oxygen and/or water in the porous structure, the surface oxidation of the nanostructures induced by heating is probable in these conditions and consequently the formation of SiO_2/Si structures. Analogous to the results from oxidized multilayer PS discussed above, quasi-ballistic electrons could also be present in the

Al/PS/Al coplanar devices after imposing high voltages on them, but their detection would be impossible in this device geometry.

Similarly to multilayer PS devices, the time dependence of the electric current after applying a constant voltage (7 V) on the Al/PS/Al devices exhibiting NDR effect evidenced telegraph noise (i.e., switching between different resistance values), as shown in Fig. 3(d). This indicates that, despite their very different structure and configuration, both types of devices display similar transport mechanisms when they are in a state exhibiting NDR behavior. Indeed, the blocking and unblocking of conduction channels outlined above could cause the telegraph noise observed in both types of devices.

For a better understanding of the physical phenomena involved in the charge transport in our PS based devices, we have studied the I-V characteristics as a function of the temperature for the Al/PS/Al devices. As shown in Fig. 4, when the temperature decreases, the NDR effect becomes less pronounced, disappearing at 223 K, as well as the hysteresis. Also, as was observed for the oxidized multilayer samples (Fig. 1(b)), the existence of stable resistance states becomes evident at 273 K. The results shown in Fig. 4 are clear evidence that, in our devices, the NDR effect is not caused by resonant tunneling. In fact, in such case the NDR peak should become more pronounced at low temperature [20]. The measured temperature dependence instead, suggests that charge trapping mechanisms are important. The disappearance of the I-V hysteresis at low temperature has been associated with freezing of traps due to their high activation energy [20, 21]. Thus, in porous silicon, the electrical transport at sufficiently low temperature is not controlled by traps because of the very large thermal emission times. Although the emission of quasi-ballistic electrons in PS at low temperature has been reported [3], this is not in contradiction with our model. We propose that the NDR effect appears in our devices due to a combination of quasi-ballistic

electron transport and trapping mechanisms, which causes Coulomb repulsion effects. In other words, without trap states available for the capture of electrons at low temperatures, the Coulomb repulsion will not occur and consequently the NDR effect will not be observed.

The interfacial or surface traps in nanostructured semiconductors are extremely sensitive to the surrounding atmosphere and in several cases the interactions between them control the transport of these materials [4, 22, 23]. In order to demonstrate that interfacial or surface traps have a determinant role in the electrical behavior of our samples, we carried out I-V curves after an intentionally breaking of vacuum, which allowed the introduction of atmospheric gases in the chamber. In Fig. 5(a), the I-V curve for a device that exhibits NDR behavior at $5x10^{-6}$ Torr is shown. Then, the vacuum was broken until reaching atmospheric pressure. In Fig. 5(b), the two first I-V curves measured consecutively at atmospheric pressure are shown. As observed for the first voltage sweep, the device no longer exhibits the NDR behavior, while the conductivity decreases as new voltage sweeps are performed, reaching values of current on the order of nanoamperes (six orders of magnitude lower than those obtained in devices that exhibit NDR). This strong decrease in conductivity may be explained by electron depletion in the crystalline silicon core due to the adsorption of oxygen or water molecules on the surface of the device. This effect associated to electronegative adsorbates has been reported in a large variety of nanostructured semiconductors [24-26]. In addition, by plotting the Log I vs. Log V (Fig. 5(c).), we found that in this state the charge transport follows the well-know space-charge limited current (SCLC) mechanism, where an ohmic behavior with a slope close to 1 for voltages lower than 7 V is observed, while for higher voltages the slope approaches a value of 2. The SCLC has been associated to a negligible density of free carriers compared to

carriers injected from the contacts [27, 28], which added to the high decrease of conductivity indicates that, effectively, the crystalline silicon structures are carrier depleted in our device due to the atmospheric adsorbates. The recovery of the NDR behavior after imposing again a vacuum of 5 x 10^{-6} Torr confirms the relevant role that surface traps have in NDR phenomena in our devices, as observed in Fig. 5(d).

In contrast to the results obtained by Lee et al. [14], our results are characterized by a noisy behavior, while the NDR peak appears at lower voltage value and it is not observed at low temperature. These differences may be caused by the SiO_2 layer present in our devices, which was removed in the work of Lee et al.. The SiO_2 plays a key role in the generation of quasi-ballistic electrons due to confinement; therefore quasi-ballistic electrons are not present in non oxidized PS devices.

As mentioned before, the NDR effect can be used to design volatile memory devices. In this kind of memories, it is possible to establish a permanent state, which will remain stable until a new state is imposed or until the power to the device is removed.

Using a device having NDR effect, with I-V characteristics like the observed in Fig. 1(a), it is possible to design volatile memories based on PS technologies. If such PS based device (PSD) is polarized with a constant current, two possible voltage values at its terminals will exist. When a voltage value greater than the maximum voltage value in the I-V curve is imposed for a short time, the device will be set in an ON state. When a voltage value lower than the maximum voltage in the I-V curve is imposed for a short time, the device will be set in an OFF state. We have experimentally verified such a device by characterizing the basic circuit shown in Fig. 6(a). A current source *I* was imposed to the PSD, while a voltage source and the switches S1 and S2 allowed selecting the logical state. Fig. 6(b) shows the logical state of switches S1 and S2. Fig. 6(c) shows the measured voltage at

terminals of PSD operating in the circuit shown in Fig. 6(a). The reproducible switching behavior of the circuit is clearly demonstrated. In addition, we have been able to build an electronic oscillator using oxidized porous silicon as a NDR device, replacing the traditional tunnel diode and the Gunn diode.

4. Conclusions

NDR effect controlled by voltage at room temperature was observed in two different PS device configurations. Experiments at different temperatures and atmospheric pressures demonstrate that carrier traps play a fundamental role in the appearance of the NDR effect. The Coulomb repulsion caused by electron trapping/detrapping was evidenced by telegraphic noise in time-dependent current at constant voltage. The combination of these results demonstrate that in PS-based devices the NDR effect is dominated by the presence of traps, which are located possibly in the SiO_2 surface or SiO_2/Si interface. Resonant tunneling mechanism is ruled out since the effect vanishes at low temperature. A simple basic circuit for memory applications showing stable switching behavior is presented. Although at the present volatile memory technology stage our device is far from optimal, it opens up an interesting venue for low-cost, easily manufactured silicon-based devices.

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Figure Captions

Figure 1. (a) NDR effect at atmospheric pressure and room temperature in Ag/ *c*-Si/SP/Ag devices. The electrode area was 28 mm^2 and the arrow indicates the progress of successive I-V curves. (b) NDR evidencing a noisy behavior in a device with an area of 0.2 mm^2. The solid lines show the multiple resistance states. (c) Time-dependent current with a constant applied voltage of 10 V for multilayer PS device after forming the NDR behavior.

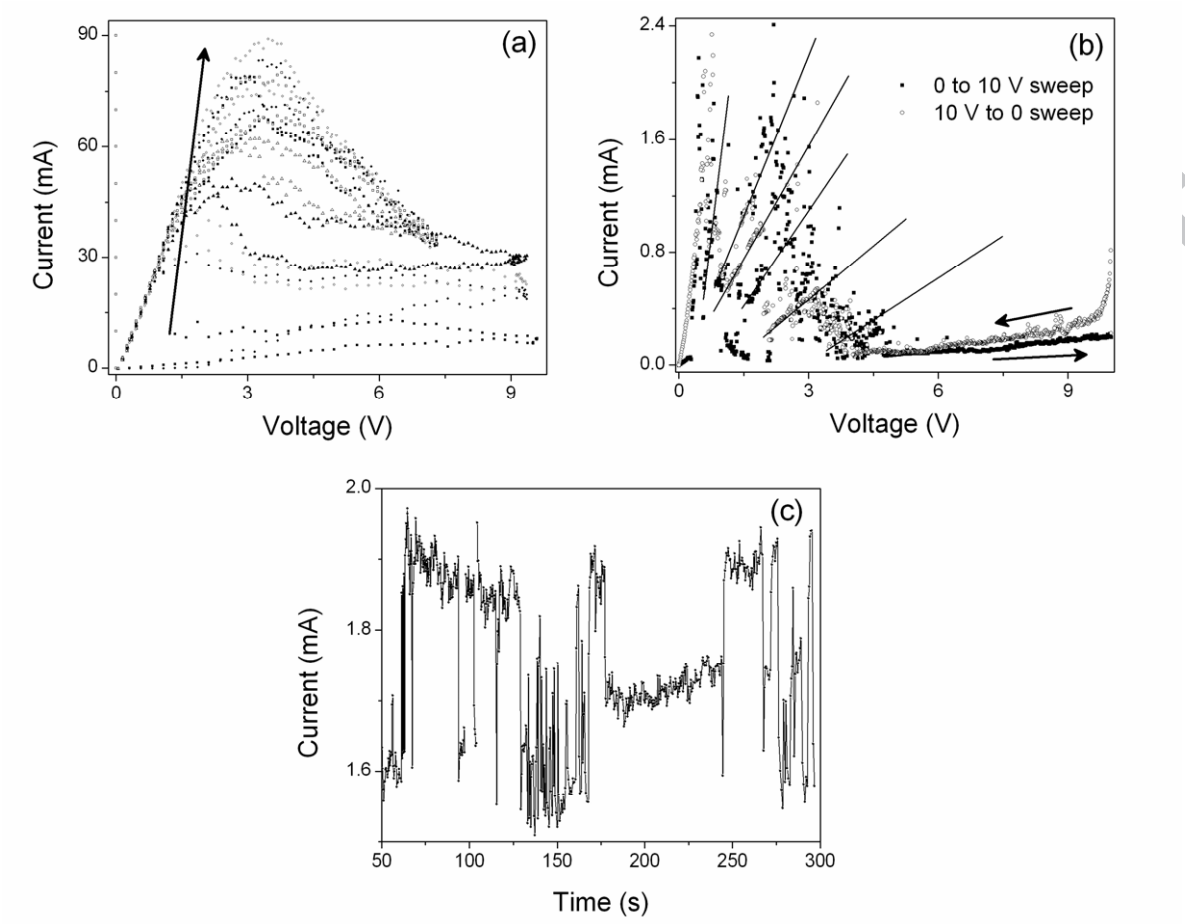
Figure 2. Current measured at collector plate indicating the existence of quasi-ballistic electrons in oxidized PS multilayer. Inset: experimental set-up.

Figure 3. (a) I-V curve in freshly made Al/PS/Al device. Inset: High conductivity state obtained after applying a high voltage. (b) Time-dependent current with a constant applied voltage of 10 V for freshly made Al/PS/Al device. (c) The NDR effect after a short-circuit for 3 hours. (d) Time-dependent current with a constant applied voltage of 7 V for Al/PS/Al device after forming the NDR behavior. In both figures (a) and (c), arrows indicate the sweep voltage direction.

Figure 4. I-V curves at different temperatures in Al/SP/Al in the state with NDR. Clearly, the NDR peak and the electrical hysteresis disappeared at low temperature.

Figure 5. I-V curves for Al/SP/Al device exhibits NDR behavior at 5 x 10^{-6} Torr (a). After the break of vacumm, the NDR behavior is not observable and the electric conductivity decrease (b). In the low conductivity state the SCLC is dominant (c). Recovery of the NDR behavior in vacuum.

Figure 6. (a) Simple circuit based on PSD for volatile memory applications. (b) Logic state for S1 and S2 switches. (c) Voltage response at the PSD terminals.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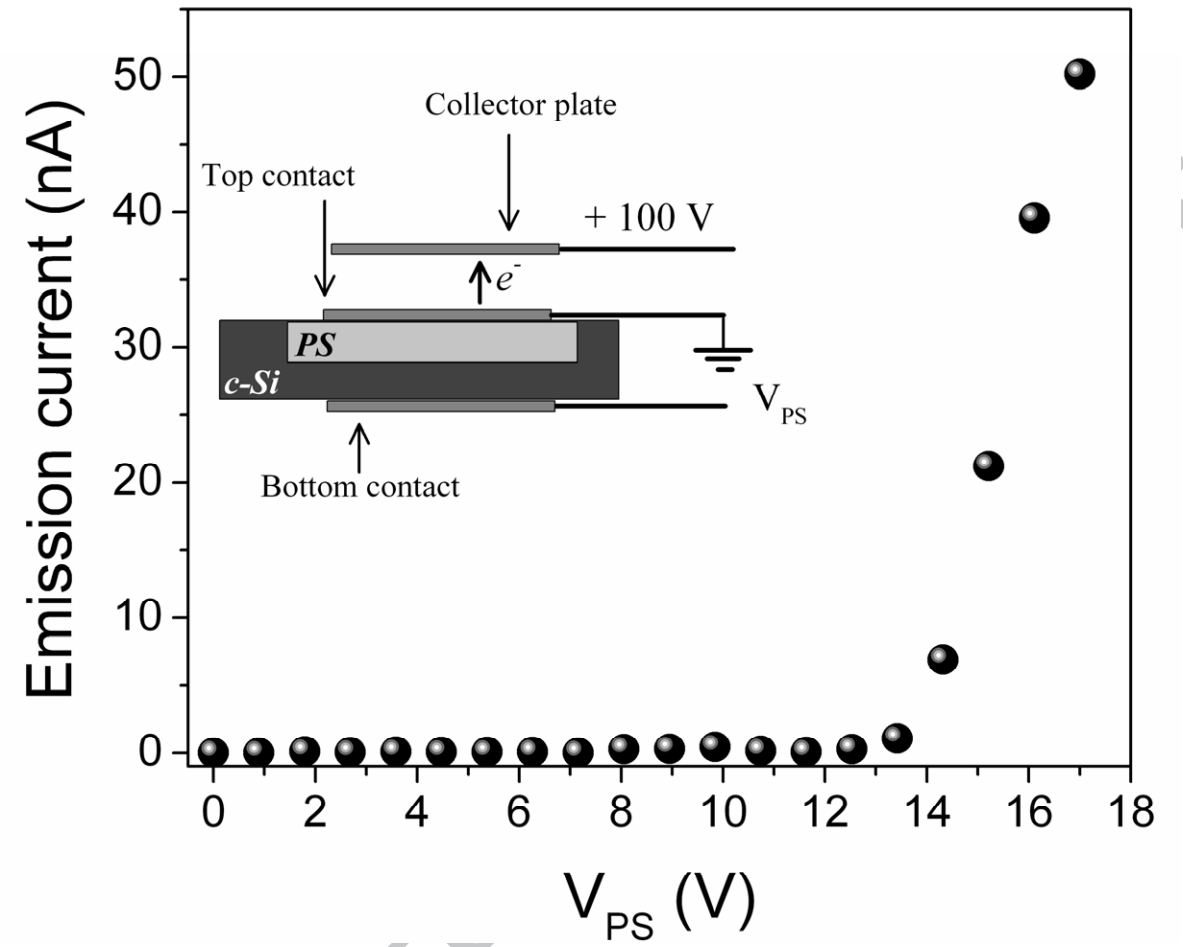
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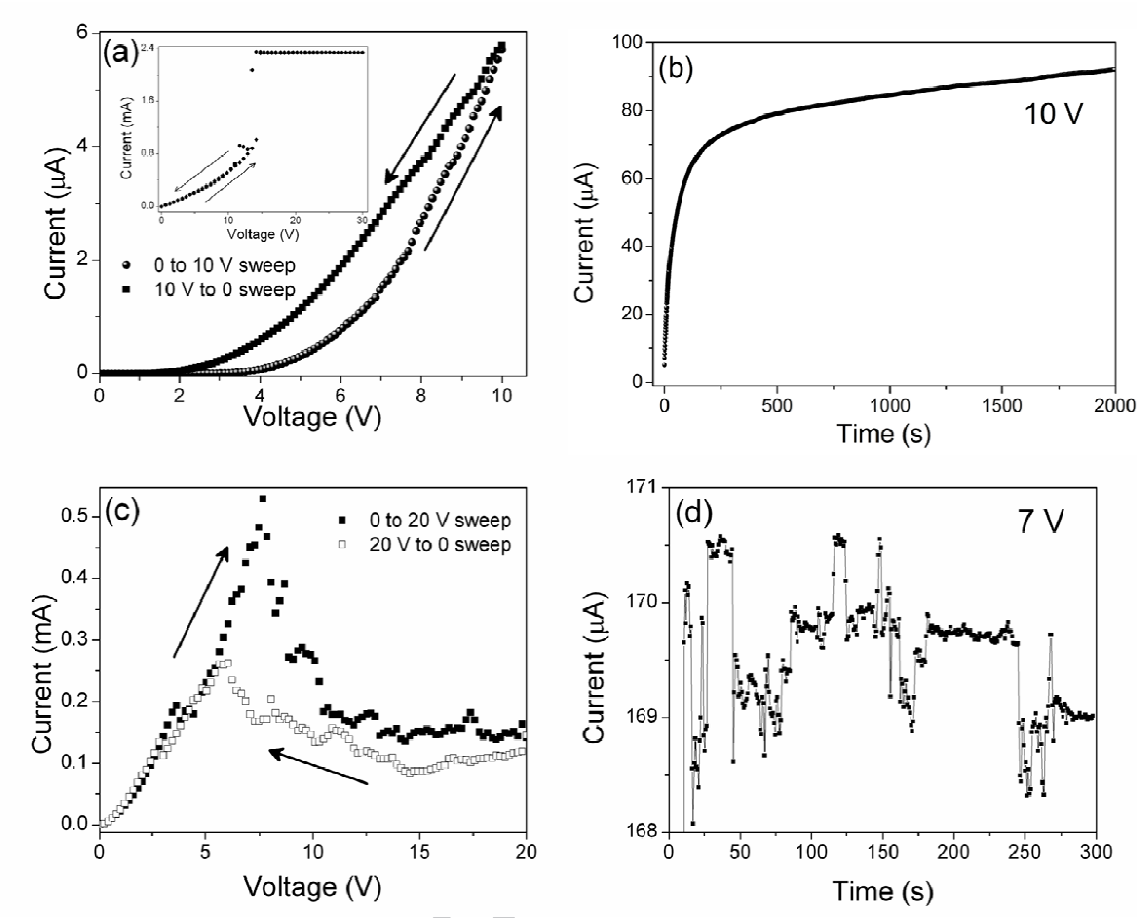

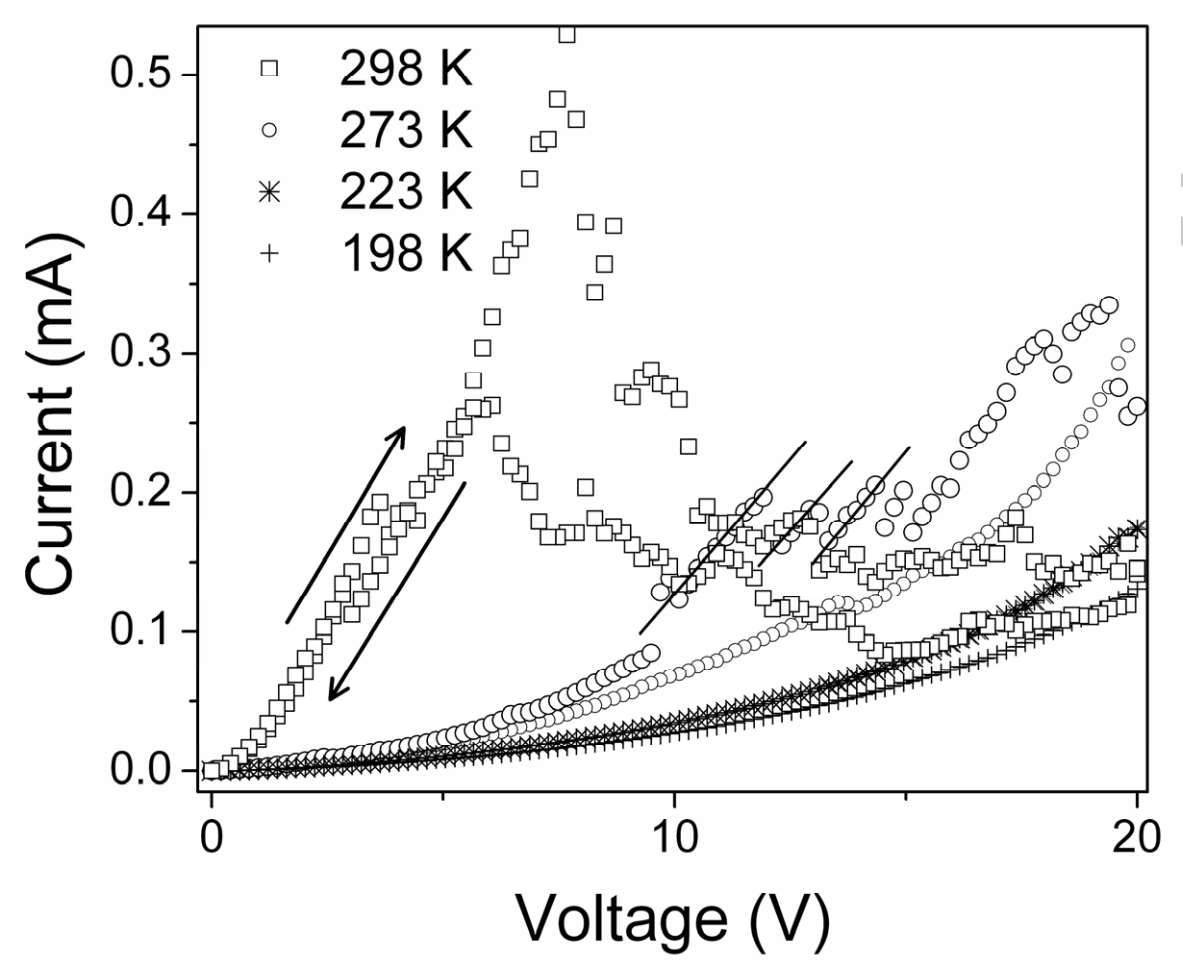
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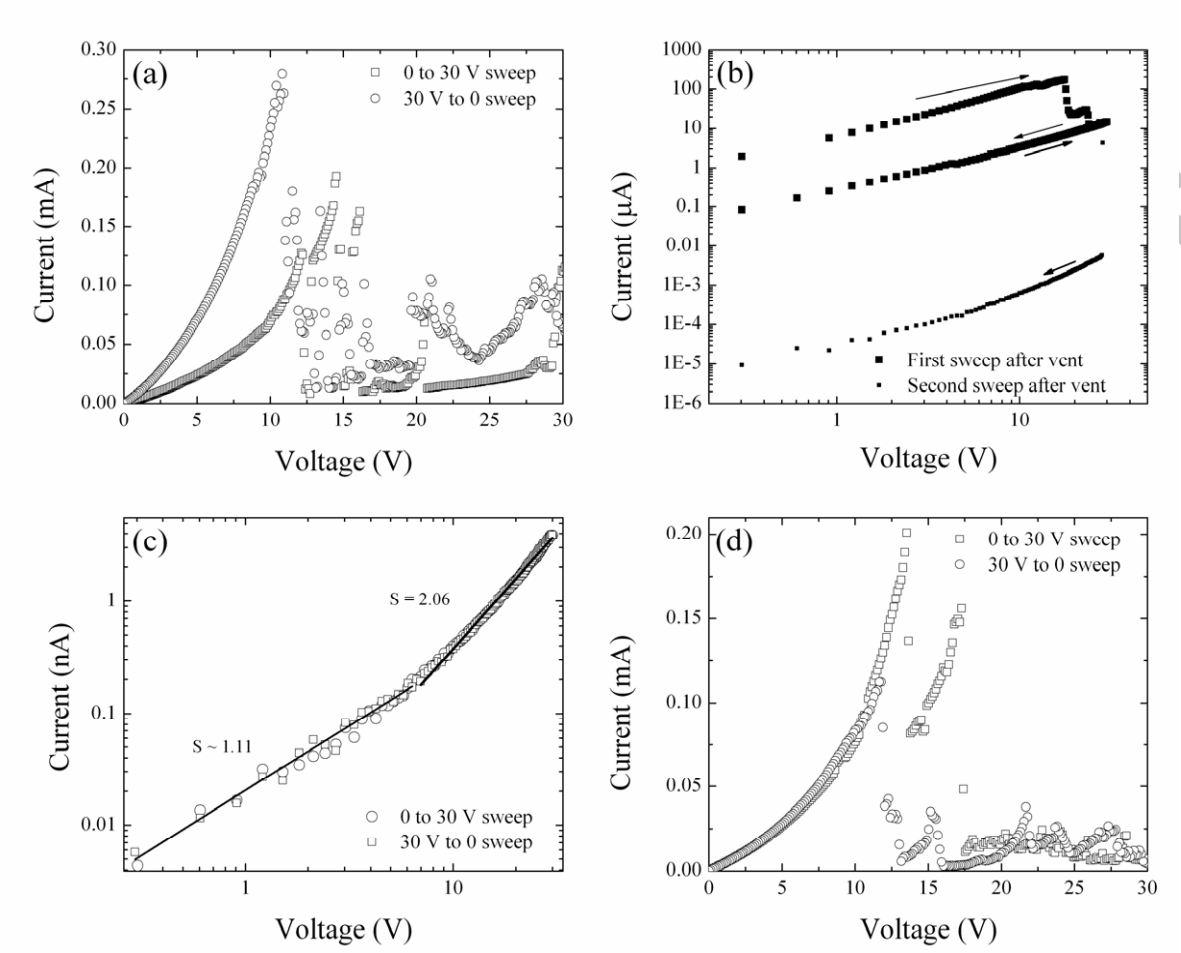
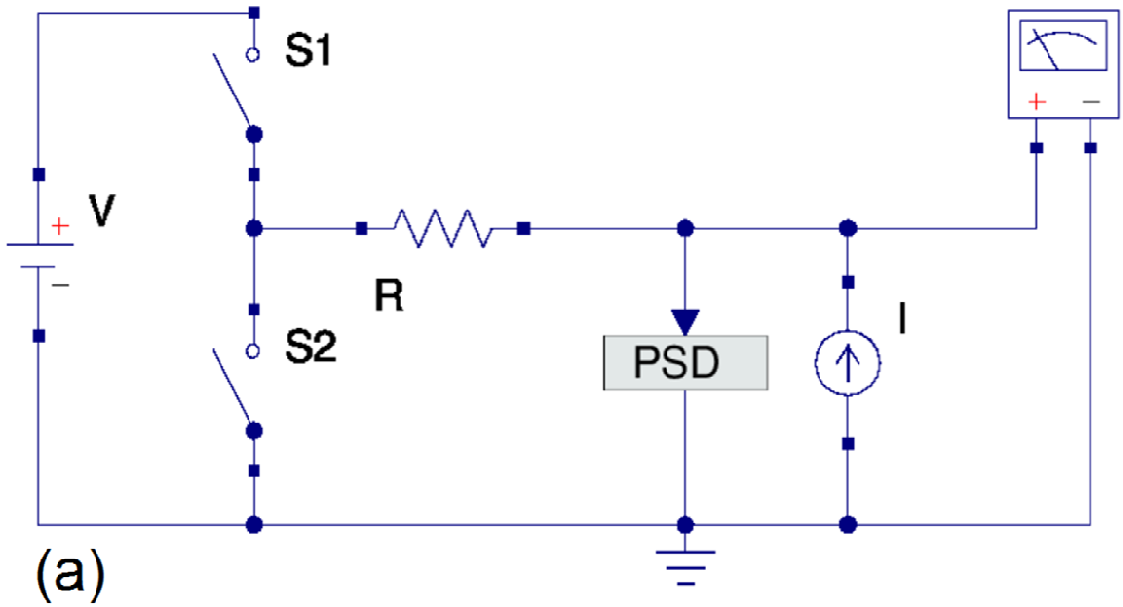
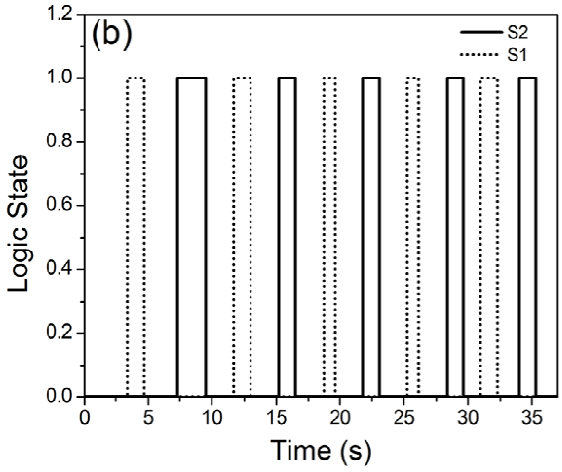
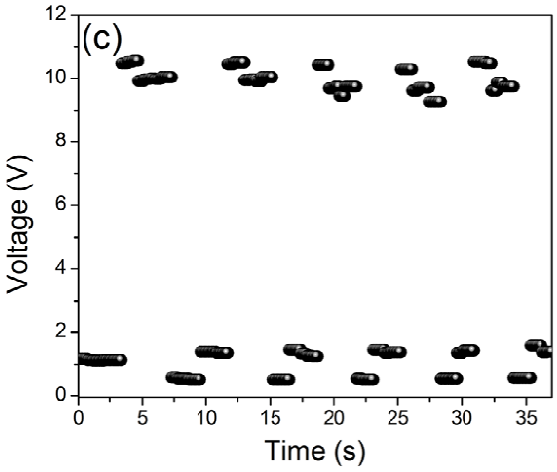
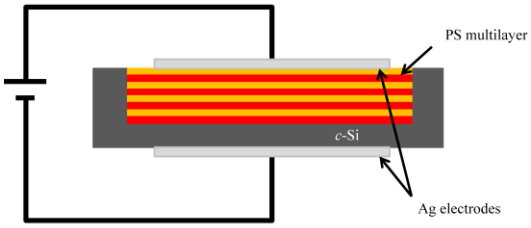


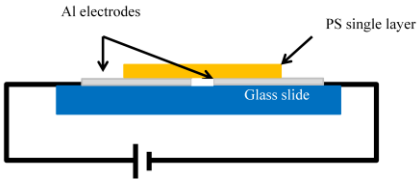






Graphical Abstract





Telegraphic noise

Negative diferential resistance

Highlights

- The NDR effect was observed in porous silicon devices at room temperature.
- Resonant tunneling is not responsible for the NDR effect in our case.
- Charge carrier traps are behind the NDR effect in our porous silicon samples.
- We present a simple circuit exploiting the NDR effect for volatile memory devices.